Claims

[c1] 1.A parallel pseudo-random binary sequence checker comprising:
circuitry capable of receiving a pseudo-random binary sequence in parallel n-bit sample, wherein said pseudo-random binary sequence is generated by a pseudo-random binary sequence generator;
circuitry capable of automatically synchronizing the state of said receiving means with an n-bit sample within said pseudo-random binary sequence to provide a next n-bit sample within said pseudo-random binary sequence; and
circuitry capable of comparing said next n-bit sample within said pseudo-random binary sequence to said next received n-bit sample within said pseudo-random binary sequence, wherein said comparing means indicates an error condition occurred if said next n-bit sample within said pseudo-random binary sequence does not equal to said next received n-bit sample within said pseudo-random binary sequence.

[c2] 2.The checker of Claim 1, wherein said checker further includes

a plurality of latches and a plurality of XOR gates connected to a subset of said plurality of latches;
circuitry capable of loading 16 most significant bits to said checker;
circuitry capable of loading 15 least significant bits to said checker; and
circuitry capable of serially advancing said plurality of latches twice.

[c3] The checker of Claim 1, wherein said checker further includes a multiplexor for yielding output bits in parallel.

[c4] The checker of Claim 1, wherein said checker further includes a mask register.

[c5] The checker of Claim 1, wherein said checker further includes an error window start register and an error window end register coupled to an error counter.

[c6] The checker of Claim 1, wherein said checker further includes a sync detect start register, a sync detect end register, a sync detect threshold register and a sync detector.

[c7] 7.A method for synchronizing a parallel pseudo-random binary sequence checker, said method comprising:
receiving a pseudo-random binary sequence in parallel n-bit sample, wherein said pseudo-random binary se-

quence is generated by a pseudo-random binary sequence generator;
automatically synchronizing the state of said receiving means with an n-bit sample within said pseudo-random binary sequence to provide a next n-bit sample within said pseudo-random binary sequence; and
comparing said next n-bit sample within said pseudo-random binary sequence to said next received n-bit sample within said pseudo-random binary sequence, wherein said comparing means indicates an error condition occurred if said next n-bit sample within said pseudo-random binary sequence does not equal to said next received n-bit sample within said pseudo-random binary sequence.

[c8] 8.The method of Claim 7, wherein said method further includes
loading 16 most significant bits to said checker;
loading 15 least significant bits to said checker; and
serially advancing said plurality of latches twice.

[c9] The method of Claim 7, wherein said method further includes providing a multiplexor for yielding output bits in parallel.

[c10] The method of Claim 1, wherein said method further includes providing a mask register for masking specific

bits in error.

[c11] The method of Claim 1, wherein said method further includes providing an error counter to count a number of errors occurred since said checker was previously reset.

[c12] The method of Claim 1, wherein said method further includes providing a logical indication of an occurrent of a failed synchronization.